Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claims 1-10 (canceled)

Claim 11 (currently amended): A process of manufacturing an integrated circuit, comprising:

forming isolation trenches in a semiconductor substrate, including:

plasma etching through a patterned hardmask layer located over a semiconductor substrate wherein said plasma etching forms a modified layer on said hardmask layer; and

removing at least a substantial portion of said modified layer by exposing said modified layer to a post plasma clean process;

forming transistor structures on and within said substrate and between said isolation trenches; and

forming interconnects within dielectric layers located over said transistor ~~transistors~~ structures that interconnect said transistor structures to form an operative integrated circuit.

Claim 12 (original): The process as recited in Claim 11 wherein said removing includes exposing said modified layer to an isotropic etch.

Claim 13 (original): The process as recited in Claim 12, wherein said isotropic etch includes phosphoric acid.

Claim 14 (original): The process as recited in Claim 11, wherein plasma etching includes etching through a patterned hardmask comprising silicon or nitrogen.

Claim 15 (original): The process as recited in Claim 11 further including removing a photoresist layer from said patterned hardmask prior to said plasma etching.

Claim 16 (original): The process as recited in Claim 11, wherein removing includes removing all of said modified layer to thereby leave an unmodified hardmask layer.

Claim 17 (original): The process as recited in Claim 11 further including forming an oxide liner in said trench.

Claim 18 (original): The process as recited in Claim 17, wherein forming said oxide liner includes forming said oxide liner prior to said removing.

Claim 19 (original): The process as recited in Claim 11 wherein exposing includes removing an upper thickness of said patterned hardmask layer ranging from about 3 nm to about 24 nm.

Claim 20 (original): The process as recited in Claim 11 wherein forming transistor structures includes forming a gate on said semiconductor substrate and forming wells and source/drain regions within said wells.